

<b>Notice of References Cited</b>	Application/Control No. 10/757,788		Applicant(s)/Patent Under Reexamination GOODING ET AL.	
	Examiner Kimberly Thornewell		Art Unit 2128	Page 1 of 1

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	B	US-			
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	K	US-			
	L	US-			
	M	US-			

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	V	Babb, Jonathan et al. "Logic Emulation with Virtual Wires." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Vol. 16 No. 6, June 1997.
	W	Tessier, Russel et al. "The Virtual Wires Emulation System: A Gate-Efficient ASIC Prototyping Environment." MIT Laboratory for Computer Science 2001.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.